iCSA/iCSL
Compact Dual Output Synthesizer

Overview and Basic Operation

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Overview

This guide describes the iCSA/iCSL Compact Dual Output Synthesizer range and explains how to select, configure, and operate the available models for RF generation and acousto-optic control applications. It covers principal operating modes, LUT-based compensation, RF power control, timing behaviour, I/O interfaces, status indicators, and supporting software.

Models

Model	Feature	Frequency Range (MHz)	RF Output Power
iCSL-**B**	USBII, III, RS232	10 – 210MHz	1.2mW
iCSA-**A**T-**B**-**C**	USBII, III, RS485, Integrated Amplifiers	**A**	**C**

A	**Frequency**	40	30 - 50 MHz
		80	60 - 100 MHz
		100	80 – 120 MHz
		120	100 - 140 MHz
		150	120 – 180 MHz
		200	150 - 250 MHz
B	**Number of Outputs**	1	RF1 only
		2	RF1 and RF2
C	**Maximum RF Power**	1	1 Watt
		2	2 Watts
		4	4 Watts
		15	15 Watts
		90	90 Watts

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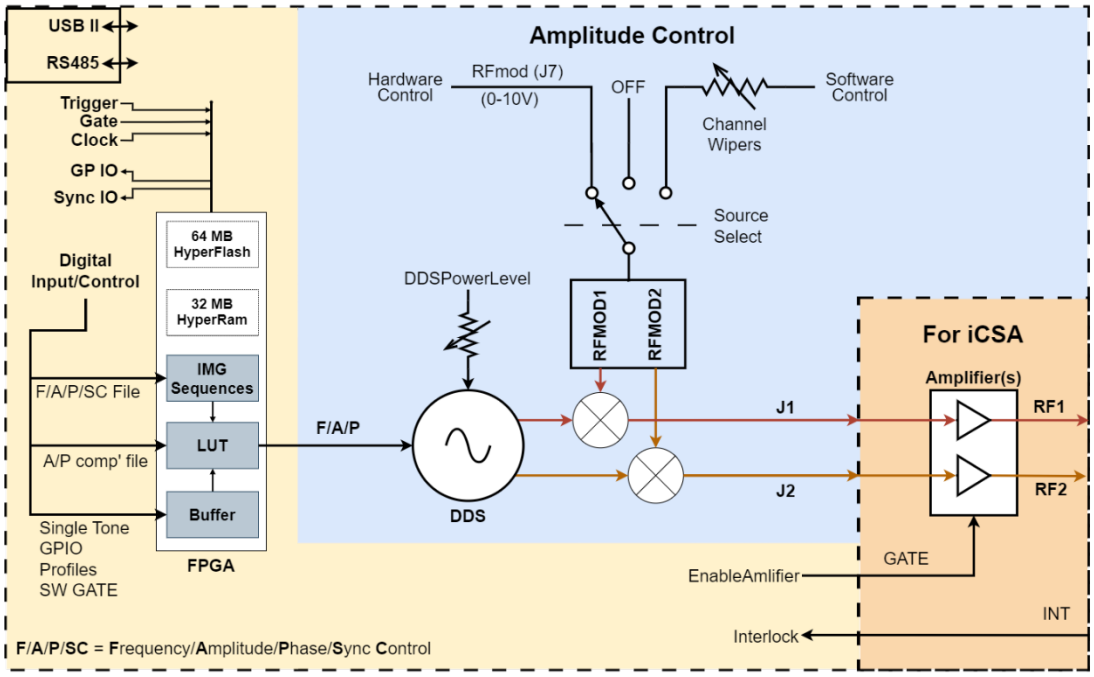
Contents

1 Hardware Overview and Key features.

The diagram below is a basic schematic of the of the compact synthesiser range. **Before** operating the device, it will be necessary to load the USB Window drivers. (See section 10).



Frequency resolution

Default standard mode = 16 bit =~ 3KHz
Precision mode = 32bts

The compact synthesizer features three basic operating modes -

1.1 Local Tone Buffer (LTB) or Single Tone Mode.

This mode is useful for setting the AO Bragg Angle or switching rapidly between 256 preassigned points. The DDS synthesizer generates a single tone output at the specified Frequency, Amplitude and Phase triad. (Abbreviation F/A/P).

Key features:

- Up to 95 KHz update rate.
- The required output tone may be selected via software control or from hardwired inputs.
- Option to bypass the LUT modifier (see LUT description below).

1.2 IMAGE or Sequence mode.

This mode is useful for generating complex scan patterns at high data rates.

Image files containing the desired frequency scan patterns are downloaded into memory space within the Compact synthesiser. Output play back is under the control of Trigger and Clock signals provided from an external system or internally generated.

Key features:

- Update rate up to 3.5MHz, (application dependent).
- Any frequency pattern may be generated e.g. random, linear, step, saw tooth.

- Multiple frequency images can be uploaded, images sequences created, appended, deleted and output order modified.
- Simultaneous upload and play of image files.
- Very large image size, in excess of 10million frequency points.

Image and Compensation LUT files (calibration files) can be generated with the supplied GUI, the C++ SDK, Python SDK or on Excel Spread sheet and imported into the C++ project.

1.3 Enhanced tone mode (Ramp / Step mode)

This mode uses the inherent sweep functions built into the DDS chip.
Frequency OR amplitude can be ramped in value.

Note: There is no dynamic control of phase or amplitude during a frequency sweep or chirp. The amplitude level remains constant during a frequency sweep duration. There is no phase control, so the benefits of using the Compensation LUT function (= AOD beam steering) cannot be applied.

1.4 Control Features

1.4.1 Look-up-table (LUT)

A calibration or compensation look-up-table (LUT) contains frequency specific phase and amplitude data. Its purpose is to compensate for non-linearity and non-uniformities in the wider system.
E.g. create efficient uniform intensity scan lines in an AOD base laser scanning system.

Initial values for the LUT are calculated and loaded into the compact synthesiser prior to running the Local Tone Buffer or Image modes. Subsequently, LUT values may be modified with real world measured data or integrated within a feedback mechanism.

1.4.2 Point Amplitude control.

Each frequency point is assigned a unique 10-bit amplitude value ranging from 0 -100% of the maximum RF power setting. This is a relative value and is dynamic i.e. able to change from output point to output point.

1.4.3 Static Power Level control.

The maximum RF output power setting is defined by *UpdateRFAmplitude* and *UpdateDDSPowerLevel* functions via digital potentiometers. These are 8-bit static controls and together define the absolute RF power level of the compact synthesiser (and any integrated power amplifier module).

- *UpdateDDSPowerLevel* applies to all four channels simultaneously.
- *UpdateRFAmplitude* is channel scoped. Each channel can have a different value.

1.4.4 Auxiliary Digital and Analog I-O signals

The Compact Synthesiser also features:

Signal Description	Ident
2 bit Synchronous output register, updated with each new image point	SDOR[0…1]
4 bits Asynchronous input/output, configurable	GPIO[1…3]
2x Synchronous analog outputs, 0 - 2.5V full scale	AOUT_Frq …Amp

2 Main operating modes and functions.

Please refer to the application program interface (API) documentation with the software development kit (SDK) available as a download.

2.1 Single (Set Calibration) Tone.

Simplest mode.
Direct programming of the DDS frequency, amplitude and phase values.
Bypasses LUT compensation.

2.2 Local Tone Mode

The Local tone buffer (LTB) area contains a maximum 256 F/A/P locations.
The 256 F/A/P Tones may be rapidly addressed using 8x external LTB address lines or directly from the operating software.

LTB ext'l address, J7 (pins 5, 6, 8, 9, 11, 12, 16, 17).	Function	Update rate
0 h ... FF h	Select Tone address	10.5usec

The compensation look-up-table (see below) may be applied to the Tone Buffer output if required.

2.3 Enhanced Tone Mode (Ramp / Step mode)

This mode uses the inherent sweep functions built into the DDS chip allowing frequency, amplitude or phase to be ramped in value. However, an internal limitation in the DDS chip prevents amplitude ramps in the Enhanced tone mode. Therefore, only frequency ramps and steps will be described.

2.3.1 Ramp Mode

A ramp or chirp is generated by rapidly incrementing the frequency. The number of increment steps and duration of the ramp are user programmable. Each output can be programmed with different ramp parameters.

The ramps are initiated from the GUI or applying a signal to the external Profile inputs on connector J7.

Available functions:
- Independent Up - Down ramp slopes.
- Dwell (stop at end value) or no-dwell (return to start value) at end of sweep duration.
- Set amplitude value for ramp. (remains constant for the ramp duration).

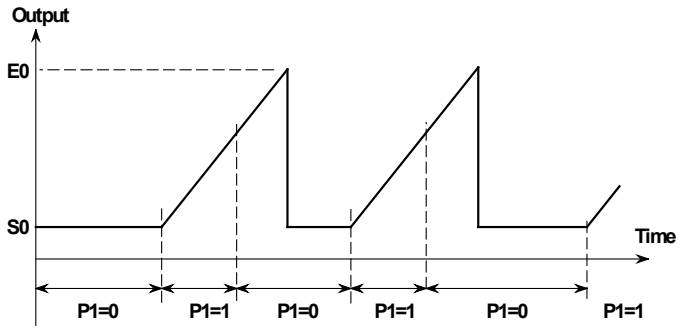
The Ramp mode offers the fastest frequency sweep capability, with a minimum dwell time of 8nsec per frequency increment.

Independent sliders for each of the four output channels define:
- Duration of the rising slope increment.
- Duration of the falling slope increment.
- The number of points for each ramp, up or down.

The falling slope only applies if 'Dwell' is selected in the ***Mode*** pull down menu.

A **Frequency Sweep no dwell** immediately returns to the start value after the end value has been reached

A ***No-Dwell*** sweep immediately returns to ***Start*** slider value (S0) after the ***End*** slider value (E0) has been reached.



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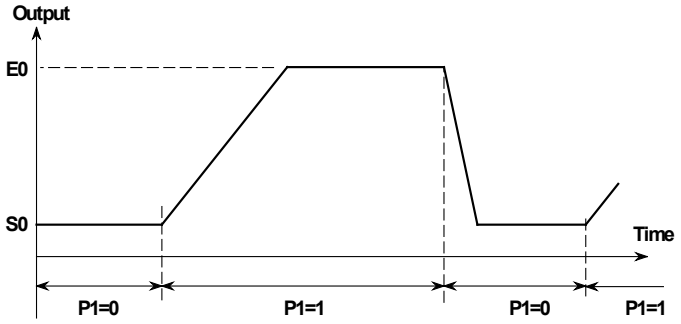
A **Frequency Sweep Dwell** only returns to the start value after a falling edge transition on the appropriate profile input.

A ***Dwell*** sweep only returns to the ***Start*** slider value (S0) after falling edge transition on the appropriate profile input.



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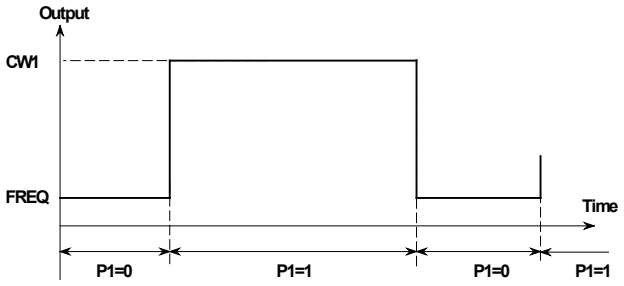
Both plots show a ramp on output J2, controlled using input P1 (on connector J7).

2.3.2 Step mode

This is essentially a two-level sweep or two-level modulation.
Step mode may be applied to the Frequency, Amplitude or Phase.
Dwell/No dwell has no function.

Plot shows a frequency step sweep controlled using input P1.
FREQ = Start Value
CW1 = End Value



2.3.3 Amplitude

The amplitude level across a Frequency or Phase sweep (or step) remains a constant.
The value is set by a combination of the *DAC Current* level buttons (Full , ½, ¼, ⅛) and the sliders on the *Signal Path* panel.

3 Image Mode.

An Image contains multiple F/A/P data points pre-arranged to give the desired frequency or scan pattern. Image playback is initiated with the Image Trigger. The output update rate is determined by the Image Clock. The Image trigger and clock may be software generated or applied from external sources. At each clock edge, the next location in the Image Memory area is addressed. The frequency and amplitude data point are read and modified by the LUT data (see below). The resultant F/A/P triad is routed to the DDS registers. An update clock is then issued to the DDS and both RF outputs are simultaneously updated* with a new Frequency, Amplitude and Phase value. Any programmed Synchronous control data will also be updated on the appropriate I/O port.

Multiple images can be grouped together into a play sequence. Each image within a sequence can have unique properties such as clock rate and post image delay. Likewise multiple sequences can be defined and queued. These are uploaded into the iMS DDR memory and played in FIFO order. Memory is dynamically allocated to permit flexibility in the size and number of both the images and sequences, and to allow simultaneous upload and output of data.

4 Look-up-table (LUT).

The LUT is frequency-addressed look-up-table for applying amplitude and phase compensation to the RF signal output. The tables are indexed by the nearest programmed LUT frequency to the demanded output frequency. Table entries are linearly spaced in frequency from the lowest to highest supported. The number of entries in the table is hardware specific. At a minimum, the LUT must contain amplitude compensation data over the desired frequency range of interest.

LUT Size: 2047 entries equally spaced from 10 – 225MHz.

Primary features: Frequency dependent compensation data:

- Amplitude: a value between 0 and 100% for modifying the output amplitude according to frequency. Used for compensating variations in AO efficiency and/or power amplifier gain.

- Phase: 0 - 360 degrees. Value represents the phase offset between adjacent channels. Typically applied to beam steered (= phased array) AO deflector designs. Channel 1 is the reference and unmodified. Channel 4 will exhibit the largest phase differential relative to Ch 1.

Secondary features: Synchronous output data:

- Sync Analog: A value between 0.0 and 1.0 that can be output on one of the synchronous DAC outputs (J7). Updated in step with the specified output RF frequency(s).

- Sync Digital: A binary value that can be output on the synchronous digital outputs. Updated in step with the specified RF output frequency(s).

(* disregarding Image Clock Delay function)

The Isomet Studio GUI released with SDK v1-7-0 onwards provides a Compensation Function to generate and optimize LUT files. Default LUT files are provided on our website.

5 RF power Level and Modulation.

The output RF power at each frequency is determined by the combination of static controls and point specific amplitude data value.

5.1 Static Asynchronous Controls.

Applies to all operating modes.

Purpose: To set the maximum safe operating RF power level.

a: ***DDS Power Level***. 8-bit non-volatile digital pot. Always programmed. Sets the DDS chip output level using a dedicated digital pot. Common to all outputs.

Typical values written and stored to DDS = 50 – 90%

<< and >>

b: Channel Specific ***RF Amplitude Control Source***. A control signal source for the RF mixers fitted on each channel. Must select and apply one.

01: CH-WIPER 1 (2). An internal 8-bit non-volatile digital pot, one per RF channel. ***00***: EXTERNAL signals*, one per RF channel, output proportional to applied control voltage.

Typical values written and stored to CH-Wipers = 50 – 100%

The above controls should be set in combination so that the AO device is operated at optimum efficiency without saturating the connected power amplifiers and/or applying excessive RF power to the AO device. Starting values will be provided on the appropriate test data sheets.

(* Can be wired together to combine multiple channels onto a common control input.
0-10V, 600-ohm / channel. May also be used for fast asynchronous amplitude modulation).

5.2 Dynamic Synchronous Control.

Purpose: To dynamically control the RF power level up to the maximum level defined by the Static Asynchronous Controls (above) according to the output frequency. E.g. to control the diffracted laser intensity at a specific scan angle.

a: Tone Buffer mode

The 10-bit amplitude data value associated with a specific frequency value. This is multiplied by the LUT amplitude calibration factor for that frequency point.

<< or >>

b: Image mode

The 10-bit amplitude data value associated with a specific frequency value. This is multiplied by the LUT amplitude compensation factor for that frequency point.

For a typical AO scanning application, the Image amplitude data is a simple "On" or "Off" value. The LUT is programmed with the variable amplitude compensation data that creates the desired weighting for the scan intensity profile.

In both cases, the LUT can be bypassed if required. The LUT is applied by default.

6 Technical Specifications.

6.1 Image Mode

Timing	Value	Condition
Frequency Settling Time	One cycle at output frequency.	Step change in Image data value. Phase accumulator re-sync = OFF (default)
	< 40nsec	Step change in Image data value Phase accumulators resync = ON Initiated every clock update
Pipeline delay: Image Clock to output	1.2usec	
Minimum Trigger to Clock edge	10nsec	
Maximum Image Clock rate	4.8MHz	LUT Compensation disabled*
	3.6MHz	Two independent outputs. LUT enabled.
Minimum Image Clock rate	16Hz	Internal trigger
	0Hz	External trigger

*Compensation can still be applied by modifying Image file data prior to download with frequency dependent phase and amplitude weighting.

GATE, TRIGGER, CLOCK inputs. J9, J10, J11	Value	Condition
Absolute Maximum Input Voltage	5.5V	
Recommended Input Voltage	3V < Vh < 5V	Vh = Logic High
Minimum Input Voltage	0V	

Active edge of the external Clock or Trigger inputs is user programmable. Default = rising

6.2 Local Tone Buffer Mode, J7

Timing	Value	Condition
Frequency Settling Time		See Image mode values
Output Delay - LTB address change	6usec	
Maximum LTB address rate	900KHz	
Minimum LTB address rate	0 Hz	

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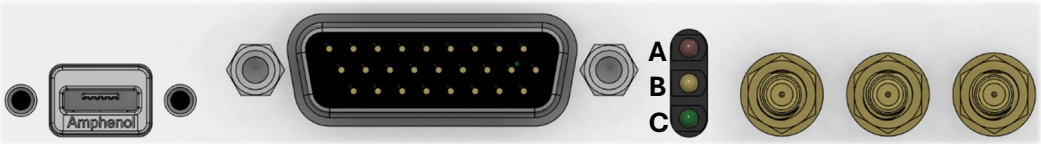
LTB address, input Voltages	Value	Condition
Absolute Maximum Input Voltage	5.5V	
Recommended Input Voltage,	3V < Vh < 5V	Vh = Logic High
Minimum Input Voltage	0V	
Isolated, signal source sink current	4mA	Per input

6.3 External Modulation Inputs, J7

Parameter	Value	Condition
RF output Rise time	< 40nsec	Step change in external modulation input
Output Delay - Modulation input	50nsec	Step change in external modulation input
Absolute Maximum Input Voltage	12V	per input.
Recommended Input Voltage	10V	
Minimum Input Voltage	0V	
Input impedance	~600Ω	per input
On:Off ratio	> 35dB	Full range
Maximum modulation rate	10MHz	
Minimum modulation rate	0 Hz	

7 LED Indicators.

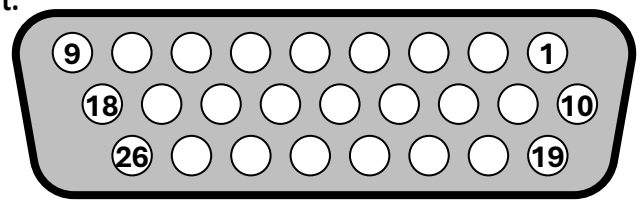
The individual functions of the tricolour led stack on the compact synthesiser are completely configurable. The following details are that of the default configuration



Ident	LED	Mode	Compact synthesiser
A	RED	If illuminated	Interlock open
B	Yellow	If illuminated	Gate satisfied (amplifiers enabled)
C	Green	Pulsing	Controller OK

8 J7, 26 way high density-D connector pinout.

D-type pin idents looking into the female 26-way connector on compact synth



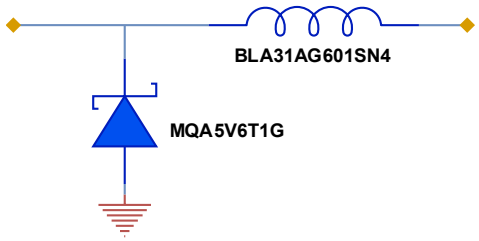
Connection for auxiliary I-O signals

Signal Designation	Signal	Type	Description	Alternate use	Pin
A Amp	Out	Analogue	Proportional to amplitude level		10
A Freq	Out	Analogue	Proportional to tuned frequency		19
RF Mod 1	In	Analogue	External modulation (0-10V)*		1
RF Mod 2	In	Analogue	External modulation (0-10V)*		2
Profile 1	In	Logic	Programmable register address	LTB0	5
Profile 2	In	Logic	Programmable register address	LTB1	6
Profile 3	In	Logic	Programmable register address	LTB2	8
Profile 4	In	Logic	Programmable register address	LTB3	9
GPIO 1	In/Out	Logic	Async general purpose input/output	LTB4	11
GPIO 2	In/Out	Logic	Async general purpose input/output	LTB5	12
GPIO 3	In/Out	Logic	Async general purpose input/output	LTB6	16
GPIO 4	In/Out	Logic	Async general purpose input/output	LTB7	17
SDOR 1	OUT	Logic	Sync-Digital Output bit 0		14
SDOR 2	OUT	Logic	Sync-Digital Output bit 1		15
Reset	In	Logic	Active high to reset		4
GND (0V)	DC				3, 7, 13, 18, 20, 21, 24
RX-P	In	Logic	RS485 receive+		22
RX-N	In	Logic	RS485 receive-		23
TX-P	Out	Logic	RS485 transmit+		25
TX-N	Out	Logic	RS485 transmit-		26

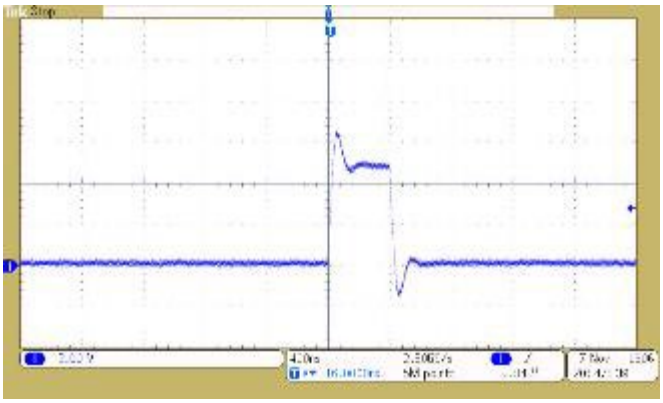
* Options available: 0-1V, 0-5V, On-Off digital,
RF_mod1 and RF_mod2 can be wired together for common control

Filter Circuit details for inputs / outputs on J7 connector

Input high voltage >3.5V, Input low voltage <0.8V
Input/output circuit for logic inputs e.g. GPIO, Profile, SDOR

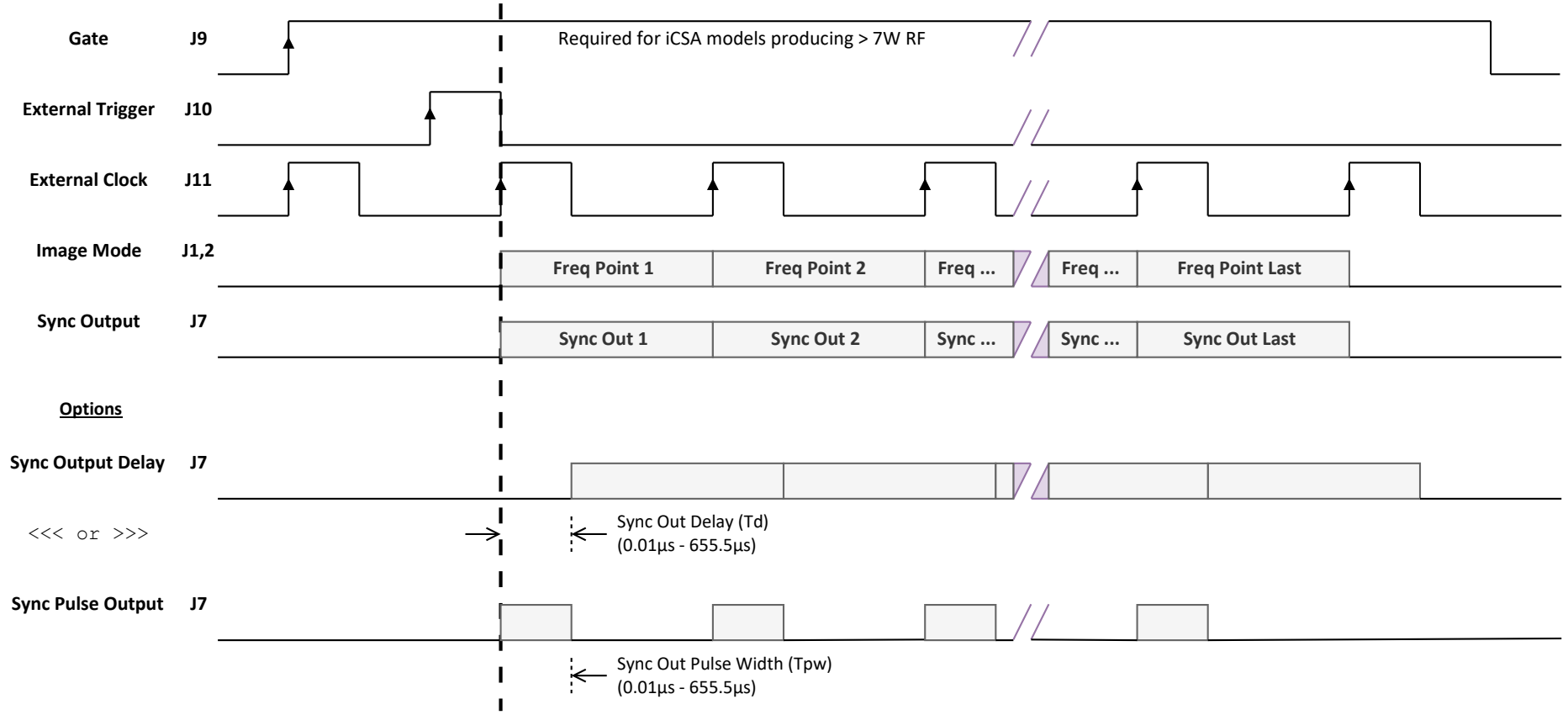


SDOR output trace at 2.5MHz Image clock rate
SDIO bits 0..11 are actively driven high. No pull-up resistor required.
DO NOT short outputs to 0V or 5V



9 Signal Timing Diagram

Applies to Image mode.



NOTE: For clarity, the 1.2usec latency between the External clock and the respective Output frequency point is not shown. This is a pipeline delay and does not impact on Image Clock rate.

NOTE: J10 & J11 can be configured for either rising or falling edge detection.

10 Extended features index

Feature	Description	App Note
Duty Cycled Output	Duty cycling the RF output to match pulsed lasers allows for higher peak RF power and lower average power.	AN0824 Drive Power Duty Cycle
Sequences	Sequences let the device play multiple stored images in order with controllable timing, looping, and reusable queue behaviour.	AN240712 iMS4 Sequence Tables
Direct programming of the DDS	Direct, low-level control of the AD9958 to access advanced frequency, phase, and amplitude features beyond the standard API.	AN26242-Programming_the_DDS_Chip

11 Software.

The Compact synthesiser is controlled using the Isomet iMS SDK which is available for a range of platforms including C++, C#, and Python and if available for both windows and Linux based systems. Isomet provides the iMS studio application for basic testing and tuning.

For more information see:

- AN26241 – iMS SDK

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